AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A high-speed transmission system having a low latency, comprising:

a plurality of first transmitter circuits in a send side; and

a plurality of first data processing circuits in a receive side ~~respectively~~, said first transmitter ~~circuit~~ circuits and said first data processing circuits ~~having been~~ connected ~~one to one~~ one-to-one via a transmission line,

wherein, so as to regulate a Delay Locked Loop (DLL) circuit (620) that regulates a timing of a sampling clock of a data signal of said first data processing circuit (600), a second transmitter circuit (300), a transmission line (900), and a second data processing circuit (700) are provided, and

wherein, when a second specific signal string ~~was~~ has been sent, a regulation start signal is caused to be distributed from said second data processing circuit (700), and

wherein said regulation is caused to be made for said DLL circuit (620) by a regulating signal string, and

wherein data starting with a bit next to a first specific signal string detected in a data signal for which a serial-parallel conversion was made is written into a FIFO circuit (660), and simultaneously, a read address synchronized with a system clock (CLKSYS) is generated from a third specific signal string that came to said second data processing circuit (700), and

whereby recovery is made for data.

2. (Currently amended) The high-speed transmission system having a low latency according to claim 1, wherein a clock for transmission having ~~a~~ an n/2 multiple frequency, which ~~was~~ is synchronized with a system clock (CLKSYS), is distributed from a first analogue Phase Locked Loop (PLL) circuit (100) to said first data processing circuit (600) and said second data processing circuit (700) via a driver (140), a transmission line (1000), and a receiver (540), said clock for transmission being distributed to said first transmitter circuit (200) and said second transmitter circuit (300).

3. (Currently amended) A high-speed transmission system having a low latency and comprising a plurality of first transmitter circuits in a send side and a plurality of first data processing circuits in a receive side respectively, said first transmitter circuit and said first data processing circuits ~~having been~~ connected ~~one to one~~ one-to-one via a transmission line, said high-speed transmission system comprising:

a plurality of first transmitter circuits (200) ~~including~~ each comprising:

~~a~~ an n(a multiple of 2)-bit register (210) that receives input data with a system clock (CLKSYS), with which ~~the above~~ input ~~parallel~~ data ~~was~~ is prepared by splitting an input parallel data~~, or~~ and receives a clock having ~~the~~ a same frequency as that of the ~~above~~ system clock (CLKSYS); and

parallel-serial conversion circuits (220 and 230) that convert a parallel data signal that is output ~~of~~ from said n(a multiple of 2)-bit registers (210) into a serial data signal, using a clock for transmission having an n/2 multiple ~~frequency,~~ frequency which ~~was~~ is synchronized with the system clock (CLKSYS), or a divided clock of said clock, for ~~transmission;~~ transmission, such that,

when an invalid data string, a regulation signal string that changes surely into 1 and 0, and a first specific signal string comes out at a free or a certain period from said first transmitter circuit (200), so that start times of the invalid data string and a second specific signal string become same and ~~the~~ finish times of the first specific signal string and a third specific signal string become same, a regulation controlling logic circuit (400) ~~that~~ generates the second specific signal string, the regulation signal string that changes surely into 1 and 0, and the third specific signal string;

a second transmitter ~~circuits~~ circuit (300) ~~including~~ comprising:

an n-bit register (310) that receives an output signal of said regulation controlling logic circuit (400) with the system clock (CLKSYS) or a clock having ~~the~~ a same frequency as that of the ~~above~~ system clock (CLKSYS); and

parallel-serial conversion circuits (320 and 330) that convert a parallel data signal that is an output of ~~this~~ said n-bit register (310) into a serial data signal, using, for transmission, a clock for transmission having an n/2 multiple frequency, ~~which was~~ synchronized with the system clock (CLKSYS), or a ~~de-multiplyed~~ de-multiplied clock of said clock ~~for transmission~~;

said plurality of first data processing circuits (600) ~~including~~ each comprising:

a DLL circuit (620) that makes a phase comparison between an output of the DLL circuit (620) that sets at an input the clock for transmission having ~~a~~ an n/2 multiple frequency of the system clock (CLKSYS) synchronized to the clock for transmission used in said first transmitter circuits (200), and a serial data signal from one of said first transmitter circuits (200) to regulate a sampling ~~lock~~ clock so as to have a timing at ~~the~~ a center of data;

sampler and serial-parallel conversion circuits (630 and 640) that sample a serial data signal from the sampling clock to convert it into a parallel data signal;

a first start-aligned detection circuit (650) that resets a regulation control signal (strt) indicating a regulation start and a regulation finish of said DLL circuit (620) when the regulation start signal comes out, releases a hold of a flip-flop that stored a lead bit position, compares the first specific signal string with a parallel data signal that ~~is output of~~ are outputs from said serial parallel conversion circuits (630 and 640) that sets the regulation control signal (strt) in ~~the~~ an event that they accorded when the regulation control signal (strt) was reset, and stores and holds ~~the~~ a lead bit position;

an alignment circuit (650) that invalidates an output with ~~the~~ a regulation control signal (strt) reset by this first start-aligned detection circuit (650), and, according to a storage result of the lead bit position of said first start-aligned detection circuit (650) when the regulation control signal (strt) was set in said first start-aligned detection circuit (650), outputs n bits, starting with a bit next to the signal string, that accorded, as data every n bits;

a write address generation circuit (661) that stops when the regulation control signal (strt) of said first start-aligned detection circuit (650) is a reset, and generates write addresses that circulate, starting with ~~the~~ an address 0 until ~~the address~~ an (m-1)th address, when it is a set;

an m-address n-bit FIFO circuit (660) that sequentially writes ~~the~~ an output of said alignment circuit (650) into ~~the~~ a designated address according to ~~the~~ an output of ~~this~~ the write address generation circuit(661);

~~a~~ an m-way n-bit multiplexer (670) that selects a data signal of the address designated by the read address written in said m-address n-bit FIFO circuit (660), being synchronized with the system clock (CLKSYS); and

~~a~~ an n-bit register(680) that writes ~~the~~ an output of this m-way n-bit multiplexer (670);

a second data processing circuit (700) ~~that is configured of~~ comprising:

a DLL circuit (720) that makes a phase comparison between ~~the~~ an output of the DLL circuit (720) that sets at ~~the~~ an input the clock for transmission having ~~a~~ an n/2 multiple frequency of the system clock (CLKSYS) synchronized with the clock for transmission used in said second transmitter circuits ~~(300), and~~ (300) and a serial data signal from said second transmitter circuits (300), to regulate a sampling clock so as to have a sampling timing at the center of data;

sampler and serial-parallel conversion circuits (730 and 740) that sample a serial

data signal with a sampling clock to convert it into a parallel data signal;

a second start-aligned detection circuit (750) that compares ~~the~~ an output of said sampler and serial-parallel conversion circuits (730 and 740) with the second specific signal string, prepares a regulation start signal with a given pulse width indicating a regulation of said DLL circuit (720) when they accorded, distributes it to said first data processing circuit (600), resets a regulation finish signal, compares the output of said serial-parallel conversion circuits (730 and 740) with a third specific signal string, and sets a regulation finish signal when they accorded;

a synchronizing circuit (760) that synchronizes the regulation finish signal with the system clock (CLKSYS) and outputs a read address start signal at such timing that the read address start signal is output after the output of said alignment circuit (650) was written into said m-address n-bit FIFO circuit (660) and yet before ~~the~~ a next data is written into the same address in said m-address n-bit FIFO circuit (660) of said plurality of said first data processing circuits (600); and

a read address generation circuit (770) that stops when the read address start signal from this synchronizing circuit (760) is reset, and distributes the read addresses that is sequentially generated in circulation of ~~the~~ an address 0 to ~~the~~ an address (m-1), and yet simultaneously designates ~~the~~ a same address for a plurality of said m-address n-bit FIFO circuits (660) of said first data processing circuit (600) when a read address start signal from this synchronizing circuit (760) is set.

4. (Currently amended) The high-speed transmission system having a low latency according to claim 3, ~~including~~ further comprising:

a first analogue PLL circuit (100) that distributes to said first transmitter circuit (200) and said second transmitter circuit (300) the clock for transmission having ~~a~~ an n/2 multiple frequency, which ~~was~~ is synchronized with said system clock (CLKSYS), and

a second analogue PLL circuit (500) that distributes to said first data processing circuit (600) and said second data processing circuit (700) the clock for transmission having ~~a~~ an n/2 multiple frequency, which ~~was~~ is synchronized with the system clock (CLKSYS).

5. (Currently amended) The high-speed transmission system having a low latency according to claim 4, wherein, in said first analogue PLL circuit (100) and in said second analogue PLL circuit (500), the system clock (CLKSYS) in the send side and the system clock (CLKSYS) in the receive side are ~~a~~ synchronized clock signals, and the system clock (CLKSYS), or a signal having a given phase relation with the system clock (CLKSYS), or having the same or 1/k (k is an integer) frequency is set at a REF clock, ~~including~~ each said first analogue PLL circuit and said second analogue PLL circuit respectively comprising:

a voltage control-type variable frequency ~~oscillators~~ oscillator (120 and 520) that oscillates at ~~a~~ an n/2 multiple frequency;

a ~~counters~~ counter (130 and 530) that divides so that a REF clock has ~~the~~ a same frequency as that of the system clock when ~~the~~ an output of ~~this~~ the voltage control-type variable

frequency ~~oscillators~~ oscillator (120 and 520) is ~~a~~ an n/2 multiple frequency of the system clock (CLKSYS); and

a phase ~~comparators~~ comparator (110 and 510) that ~~make~~ makes a phase comparison between ~~the~~ an output of ~~these counters~~ the counter (130 and 530) and the REF clock to control a control voltage of said voltage control-type variable frequency ~~oscillators~~ oscillator (120 and 520) so that ~~the phases~~ a phase and ~~the~~ a frequency of the output of said ~~counters~~ counter (130 and 530) become equal to that of the REF clock.

6. (Currently amended) The high-speed transmission system having a low latency according to claim ~~4~~ 3, further comprising:

a first a first analogue PLL circuit (100) that distributes to said first transmitter circuit (200) and said second transmitter circuit (300) the clock for transmission having an n/2 multiple frequency, which is synchronized with said system clock (CLKSYS),

wherein, ~~in said first data processing circuit (600) and said second data processing circuit (700), is omitted the second analogue PLL circuit (500) that distributes the clock for transmission having a an n/2 multiple frequency, which was synchronized with the system clock (CLKSYS), and the~~ an output of the first analogue PLL circuit (100) in the send side is distributed to said first data processing circuit (600) and said second data processing circuit (700) via a driver (140), a transmission line (1000) and a receiver(540) as ~~the~~ a clock for transmission having ~~a~~ an n/2 multiple frequency~~, which was synchronized with the system clock (CLKSYS)~~.

7. (Original) The high-speed transmission system having a low latency according to claim 6, wherein the system clock (CLKSYS) in the send side and the system clock (CLKSYS) in the receive side are not synchronized.

8. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said first transmitter circuit (200) and said second transmitter (300) ~~includes~~ comprise:

pre-emphasis control circuits (230 and 330) that increase an output multitude of drivers (240 and 340) when a data signal is different from one that is behind one data portion, and reduce it when it is the same; and

drivers (240 and 340) that generate a data signal pre-emphasized according to ~~the~~ an output of these pre-emphasis control circuits (230 and 330), of which a pre-emphasis quantity is selectable.

9. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein each of said parallel-serial conversion circuits (220 and 230; 320 and 330) ~~include~~ comprise:

~~a~~ an n/2:1 multiplexer (220; 320) that includes a plurality of 2:1 multiplexer and registers (221) that are ~~configured~~ comprised of:

a selector (S0) that sets 2 bits of former-step flip-flops (F30 and F31) at input, sets

a clock (CK30) of the former-step flip-flops (F30 and F31) at a selection signal, selects an output of the flip-flop (F30) for a first half period of the clock (CK30), and selects an output of the flip-flop (F31) for ~~the~~ a remaining half period; and

a flip-flop (F32) having a two-multiple frequency of the clock (CK30) that samples an output of said selector (S0) with an edge of a clock (CK31) that differs in a phase from a sampling edge of the clock (CK30), said n/2:1 multiplexer (220; 320) configured to continuously connect said 2:1 multiplexer and registers (221) so as to set the former-step register in a first step at said n-bit register (210) and to set the register of said 2:1 multiplexer and registers (221) at the former-step register in a second step and more; and

a 2:1 multiplexer (230; 330) that is ~~configured~~ comprised of selectors (S40 and S41) that set at a selection signal a sampling clock (CK41) adapted so that a sampling edge of ~~the~~ last flip-flops (F40 and F41) of said n/2:1 multiplexer (220; 320) becomes a back edge, selects a positive output and a negative output of the flip-flop (F40) for a former-half period of the sampling clock (CK41), and a positive output and a negative output of the flip-flop (F42) obtained by sampling ~~the~~ an output of a flip-flop (F41) with ~~the~~ a leading edge of the sampling clock (CK41) set at a sampling edge for a latter-half period of the sampling clock (CK41).

10. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said sampler and serial-parallel conversion circuits (630 and 640; 730 and 740) ~~include~~ comprise:

a sampler and de-multiplexer (630; 730) ~~that is configured~~ comprised of:

a flip-flop (F51) that samples a serial data signal with ~~the~~ a leading edge of a sampling clock (CK1) by keeping it at ~~the~~ a center of data;

a flip-flop (F52) that samples a serial data signal with ~~the~~ a back edge of the sampling clock (CK1) by keeping it at the center of data; and

a flip-flop (F53) that samples with the back edge of the sampling clock (CK1) the output of a flip-flop (F51) sampled with the leading ~~edge; said~~ edge, said sampler and de-multiplexer (630; 730) outputting ~~the~~ two parallel data signals sampled with timing of the output unified with the back edge of the sampling clock (CK1);

a 1:n de-multiplexer (640) that is configured of a 1:4 de-multiplexer, comprising:

a 1:n/4 de-multiplexer in which 1:2 de-multiplexers (641), which obtain two parallel data of which output timing was unified with ~~the~~ a back edge of ~~the~~ a clock (CK2T), ~~were~~ are connected continuously in 0 (zero) ~~step~~ to plural steps, said 1:2 de-multiplexer comprising:

a counter (CNT61) that divides with ~~the~~ a leading edge of ~~the~~ a sampling clock (CK1);

flip-flops (F61 and F62) that ~~samples the~~ sample an output of the flip-flop sampled with ~~the~~ a back edge of ~~the~~ a former-step sampling clock (CK1), unified using ~~the~~ a leading edge and ~~the~~ a back edge of a clock (CK2T) that is ~~the~~ an output of this counter (CNT61); and

a flip-flop (F63) that samples, with the back edge of the clock (CK2T), the output of the flip-flop (F61) sampled with the leading edge of the clock (CK2T);

a counter (CNT71) that prepares a clock (CK3T) divided in half, using ~~the~~ a leading edge of ~~the~~ a sampling clock of a register (in ~~the~~ an event of the zero step, the sampler and 1:2 de-multiplexer (630)) that is each output of these 1:n/4 de-multiplexers;

a counter (CNT72) that prepares a clock (CK4T) divided in half, using ~~the~~ a back edge of the clock (CK3T);

a flip-flop (F71) that samples an input data signal with the leading edge of the clock (CK3T) for a former-half period of a clock (CK4T) and holds for a latter-half period of the clock (CK4T);

a flip-flop (F72) that samples with ~~the~~ a back edge of the clock (CK3T) for a former-half period of the clock (CK4T) and holds for a latter-half period of the clock (CK4T);

a flip-flop (F74) that samples an input data signal with ~~the~~ a leading edge of the clock (CK3T) for a latter-half period of the clock (CK4T) and holds for a former-half period of the clock (CK4T);

a flip-flop (F75) that samples with the back edge of the clock (CK3T) for a latter-half period of the clock (CK4T) and holds for a former-half period of the clock (CK4T);

a flip-flop (F73) that samples the output of the flip-flop (F71) with the back edge of the clock (CK3T); and

a flip-flop (F76) that samples the output of the flip-flop (F74) with the back edge of the

clock (CK3T).

11. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said first start-aligned detection circuit (650) ~~includes~~ comprises:

a first start-aligned conveyer circuit (651) ~~that is configured~~ comprised of:

an OR circuit (OR81) ~~that includes~~ comprising 2n conveyer circuits (CP1,..., CP2n) that compare n bits (C0, ..., Cn-1), which are a first specific signal string, with n bits starting with each bit of 2n bits (D0, ..., D2n-1) of ~~the~~ an output of said 1:n de-multiplexer (640) that is data), and applies an OR to each output of the conveyer circuits (CP1, CP2, ..., CPn) that compared a bit string that starts with lead bits (D1, D2, ..., Dn) that come to be in a latter-half period of ~~the~~ a clock (Ck4T) of 1:4 de-multiplexer (642) of said 1:n de-multiplexer (640);

an OR circuit (OR82) that applies an OR to each output of ~~the~~ conveyer circuits (CPn+1, ..., CP2+n) that ~~compared~~ compare a bit string of which the last bit of each n bits starts with lead bits (Dn+1, ..., D2n-1 and D0) that become a bit sampled for a former-half period of the clock (CK4T); and

a selector (S81) that selects ~~the~~ an output of said OR circuit (OR81) for a former-half period of ~~the~~ a clock (CK4T) and selects for a latter-half period of the clock (CK4T) that is a determination period of said OR circuit (OR82);

a start-aligned control circuit (652) comprising:

flip-flops (F81 and F82) for synchronizing a regulation start signal with the clock

(CK3T); and

a flip-flop (F83) that applies an AND to ~~the~~ a negative output of the flip-flop (F82) and ~~the~~ an output of the flip-flop (F83), and set at ~~the~~ an input a signal obtained by applying an OR to ~~its~~ an output of the AND and ~~the~~ an output of the selector (S81) of said first start-aligned conveyer circuit (651); and

a lead bit position storage circuit (653) ~~that is configured~~ comprised of:

n flip-flops with hold (R1,..., Rn) that set at ~~the~~ a data input ~~the~~ an output of the conveyer circuits (CP1, ..., CPn), fetch data for a former-half period of the clock (CK4T) and yet at ~~the~~ a time that ~~the~~ an output of said start-aligned control circuit (652) is under regulation, and holds in the other conditions;

n flip-flops (Rn+1,..., R2n) that set at ~~the~~ a data input ~~the~~ an output of the conveyer circuits (CPn+1, ..., CP2n), fetch data for a latter-half period of the clock (CK4T) and yet at the time that the output of said start-aligned control circuit (652)is under regulation, and holds in the other conditions.

12. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said alignment circuit (650) ~~is configured of~~ comprises:

an OR circuit group that applies an OR to ~~the~~ an output of a free lead bit position storage circuit (653) and ~~the~~ an output of ~~the~~ an nth-bit lead bit position storage circuit (653) from ~~the~~ a lead bit position of this lead bit position storage circuit (653);

n selectors (S91, S92,..., S9n) that select from ~~the~~ an output of the 1:n de-multiplexer (640) n bits starting with two lead bits that the output of this OR circuit group indicates, further select for a former-half period of the ~~lock~~ clock (CK4T) when the lead bits ~~is~~ are D1, ..., Dn, and select for a latter-half period of the ~~lock~~ clock (CK4T) when the lead bits ~~is~~ are Dn+1, ..., D2n and D0; and

flip-flops (F91, F92,..., F9n) that sample n bits of ~~the~~ an output of these selector (S91, S92,..., S9n) with ~~the~~ a back edge of the clock (CK3T).

13. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein, from a m-address n-bit FIFO circuit (660) comprising:

a write address generation circuit (661) that inputs a signal obtained by applying an AND to ~~the~~ negative outputs of first (m-1) flip-flops out of m flip-flops connected continuously, into a first flip-flop, and applies an INPUT and an AND to ~~the~~ a regulation control signal (strt) of said start-aligned control circuit (652) of said first start-aligned detection circuit (650) in inputting the signal into the first flip-flop or all flip-flops; and

~~a~~ an m x n FIFO (662) having ~~the~~ an address number m and ~~the~~ a bit number n that writes ~~the~~ an output of said alignment circuit (650) as ~~the~~ a data input according to ~~the~~ a write address,

said m-way n-bit multiplexer (670) fetches n-bit data written in said m x n FIFO (662) according to ~~the~~ a read address.

14. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said n-bit register (680) comprises n flip-flops (FD0, FD1, FD2, and FD3) that write ~~the~~ an output of said m-way n-bit multiplexer (670) with the system clock (CLKSYS).

15. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said second data processing circuit (700) ~~includes~~ comprises:

a second start-aligned conveyer circuit (751) ~~that is configured of~~ comprising:

an OR circuit (OR81) that includes 2n conveyer circuits (CP1,..., CP2n) that compare n bits, which are a second specific signal string, with n bits starting with each bit of 2n bits (D0, ..., D2n-1) of ~~the~~ an output of said 1:n de-multiplexer (740) that is data, and applies an OR to each output of conveyer circuits (CP1, CP2, ..., CPn) that compared a bit string starting with lead bits (D1, D2, ..., Dn), of which ~~the~~ a last bit of respective n bits comes to be in a latter-half period of ~~the~~ a clock (Ck4T) of the 1:4 de-multiplexer of said 1:n de-multiplexer (740);

an OR circuit (OR82) that applies an OR to each output of the conveyer circuits (CPn+1,, ..., CP2+n) that compared a bit string starting with lead bits (Dn+1, ..., D2n-1 and D0), of which ~~the~~ a last bit of each n bits becomes a bit sampled for a former-half period of the clock (CK4T); and

a selector (S81) that selects ~~the~~ an output of said OR circuit (OR81) for a former-half period of the clock (CK4T) and selects it for a latter-half period of the clock (CK4T) that is a determination period of said OR circuit (OR82);

a third start-aligned conveyer circuit (752) ~~that is configured of~~ comprising:

an OR circuit (OR81) that includes ~~the~~ 2n conveyer circuits (CP1,..., CP2n) that compare n bits (C0, ..., Cn-1), which are a third specific signal string, with n bits starting with each bit of 2n bits (D0, ..., D2n-1) of ~~the~~ an output of said 1:n de-multiplexer (740) that is data, and applies an OR to each output of the conveyer circuits (CP1, CP2, ..., CPn) that compared a bit string starting with lead bits (D1, D2, ..., Dn), of which a last bit of respective n bits comes to be in a latter-half period of the clock (Ck4T) of the 1:4 de-multiplexer of said 1:n de-multiplexer (740);

an OR circuit (OR82) that applies an OR to each output of ~~the~~ conveyer circuits (CPn+1,, ..., CP2+n) that compared a bit string starting with lead bits (Dn+1, ..., D2n-1 and D0), of which ~~the~~ a last bit of respective n bits becomes a bit sampled for a former-half period of the clock (CK4T); and

a selector (S81) that selects ~~the~~ an output of said OR circuit (OR81) for a former-half period of the clock (CK4T) and selects it for a latter-half period of the clock (CK4T) that is a determination period of said OR circuit (OR82); and

a regulation control circuit (753) comprising:

a flip-flop (FB4) that applies an AND to ~~the~~ an output of said second start-aligned conveyer circuit (751), and ~~the~~ an output of a plurality of flip-flops (FB2 and FB3) connected continuously that obtain ~~the~~ a negative output delayed with ~~the~~ a same output set at ~~the~~ an input, and prepares a regulation start signal that is of ~~differential~~ a pulse waveform to distribute it to all

said first data processing circuits (600); and

a flip-flop (FB1) that sets at the input a signal obtained by applying an OR to a signal obtained by applying an AND to the negative signal of the regulation start signal and the output of the flip-flop (FB1), and the output of the selector (S81) of said third start-aligned conveyer circuit (752), and prepares a regulation finish signal.

16. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said read address generation circuit (770):

sets at ~~the~~ an input of ~~the~~ a first flip-flop a signal obtained by applying an AND to ~~the~~ negative outputs of ~~the~~ first (m-1) flip-flops (FC2 to FC4) out of m flip-flops (FC2 to FC5) connected continuously;

applies an INPUT and an AND to ~~the~~ a read address start signal from a synchronizing circuit (760) in inputting a first or all flip-flops; and

distributes to all said first data processing circuits (600) ~~the~~ a prepared read address from m flip-flops (FC2 to FC5).

17. (Currently amended) The high-speed transmission system having a low latency according to claim 3, wherein said parallel-serial conversion circuits (220 and 230; 320 and 330) comprise:

~~a~~ an n/2:1 multiplexer (220; 320) comprising a plurality of 2:1 multiplexer and registers (221) ~~that are configured of~~ comprising:

a selector(S0) that sets 2 bits of ~~the~~ former-step flip-flops (F30 and F31) at ~~the~~ an input, sets ~~the~~ a clock (CK30) of the former-step flip-flops (F30 and F31) at ~~the~~ a selection signal, selects ~~the~~ an output of the flip-flop (F30) for a first-half period of the clock (CK30), and selects ~~the~~ an output of the flip-flop (F31) for ~~the~~ a remaining half period; and

a flip-flop (F32) that samples ~~the~~ an output of said selector (S0) with ~~the~~ an edge of the clock (CK31) having a 2-multiple frequency of the clock (CK30), which differs in a phase from ~~the~~ a sampling edge of the clock(CK30), said n/2:1 multiplexer (220; 320) configured to continuously connect said 2:1 multiplexer and registers (221) so as to set ~~the~~ a register in ~~the~~ a former-step of ~~the~~ a first step at said n-bit register (210), and to set the register of said 2:1 multiplexer and register (221) at the former-step in ~~the~~ a second step and more;

a 2:1 multiplexer (230; 230) ~~that is configured of~~ comprising selectors (S40 and S41) that set at the selection signal ~~the~~ a sampling clock (CK41) adapted so that ~~the~~ a sampling edge of ~~the~~ a last flip-flop (F40 and F41) of said n/2:1 multiplexer (220; 320) becomes ~~the~~ a back edge, select and output ~~the~~ a positive output and ~~the~~ a negative output of the flip-flop (F40) for a former-half period of the sampling clock (CK41), and ~~the~~ a positive output and ~~the~~ a negative output of the flip-flop (F42) obtained by sampling ~~the~~ an output of the flip-flop (F41) by setting ~~the~~ a leading edge of the sampling clock (CK41) as a sampling edge for a latter-half period of the sampling clock (CK41), and wherein said sampler and serial-parallel conversion circuits (630 and 640; 730 and 740) ~~include~~ comprise:

a sampler and 1:2 de-multiplexer (630; 730) ~~that is configured of~~ comprising:

a flip-flop (F51) that samples a serial data signal with ~~the~~ a leading edge of the sampling clock (CK1) by keeping it at ~~the~~ a center of data;

a flip-flop (F52) that samples it with ~~the~~ a back edge of the sampling clock (CK1); and

a flip-flop (F53) that samples with the leading edge of the sampling clock (CK1) ~~the~~ an output of the flip-flop (F51) sampled with the leading edge; said sampler and 1:2 de-multiplexer (630; 730) outputting two parallel data signals sampled by unifying the timing of the output with the back edge of the sampling clock (CK1); and

a 1:n de-multiplexer (640) ~~that is configured of~~ comprising a 1:4 de-multiplexer (642) comprising:

a 1:n/4 de-multiplexer in which 1:2 de-multiplexers (641) were continuously connected in 0 (zero) ~~step~~ to plural steps, said 1:2 de-multiplexer (641) comprising:

a counter (CNT61) that divides with a leading edge of the sampling clock (CK1);

flip-flops (F61 and F62) that sample the output of the flip-flop sampled by unifying with the back edge of the former-step sampling clock (CK1), using the leading edge and the back edge of the clock (CK2T) that is the output of this counter (CNT61); and

a flip-flop (F63) that samples with the back edge of the clock

(CK2T) the output of the flip-flop (F61) sampled with the leading edge of the clock (CK2T), said 1:2 de-multiplexer (641) obtaining two parallel data signals of which the timing of the output was unified with the back edge of the clock (CK2T);

a counter (CNT71) that prepares a clock (CK3T) divided in half, using the leading edge of the sampling clock of the register (in the event of zero step, the sampler and 1:2 de-multiplexer (630)) that is each output of this 1:n/4 de-multiplexer;

a counter (CNT72) that prepares a clock (CK4T) divided in half, using the back edge of the clock (CK3T);

a flip-flop (F71) that samples ~~the~~ input data signal with ~~the~~ a leading edge of the clock (CK3T) for a former-half period of the clock (CK4T) to hold for a latter-half period of the clock (CK4T);

a flip-flop (F72) that samples with ~~the~~ a back edge of the clock (CK3T) for a former-half period of the clock (CK4T) to hold for a latter-half period of the clock (CK4T);

a flip-flop (F74) that samples ~~the~~ input data signal with the leading edge of the clock (CK3T) for a latter-half period of the clock (CK4T) to hold for a former-half period of the clock (CK4T);

a flip-flop (F75) that samples with the back edge of the clock (CK3T) for a latter-half period of the clock (CK4T) to hold for a former-half period of the clock (CK4T);

a flip-flop (F73) that samples the output of the flip-flop (F71) with the back edge of the clock (CK3T); and

a flip-flop (F76) that samples the output of the flip-flop (F74) with the back edge of the clock (CK3T), and where said first start-aligned detection circuit (650) ~~includes~~ comprises:

a first conveyer circuit (651) ~~that is configured of~~ comprises:

an OR circuit (OR81) that includes 2n conveyer circuits (CP1,..., CP2n) that compare n bits (C0, ..., Cn-1), which are a first specific signal string, with n bits starting with each bit of 2n bits (D0, ..., D2n-1) of the output of said 1:n de-multiplexer (640) that is data, and applies an OR to each output of the conveyer circuits (CP1, CP2, ..., CPn) that compared a bit string starting with lead bits (D1, D2, ..., Dn), of which ~~the~~ a last bit of respective n bits comes to be in a latter-half period of the clock (Ck4T) of 1:4 de-multiplexer (642) of said 1:n de-multiplexer (640);

an OR circuit (OR82) that applies an OR to each output of the conveyer circuits (CPn+1,, ..., CP2+n) that compared a bit string starting with lead bits (Dn+1, ..., D2n-1 and D0), of which ~~the~~ a last bit of respective n bits becomes a bit sampled for a former-half period of the clock (CK4T); and

a selector (S81) that selects ~~the~~ an output of said OR circuit (OR81) for a former-half period of the clock (CK4T) and selects for a latter-half period of the clock (CK4T) that is a determination period of said OR circuit (OR82);

a start-aligned control circuit (652) comprising:

flip-flops (F81 and F82) for synchronizing ~~the~~ a regulation start signal with the clock (CK3T); and

a flip-flop (F83) that applies an AND to ~~the~~ a negative output of the flip-flop (F82) and ~~the~~ an output of the flip-flop (F83), and sets at ~~the~~ an input a signal obtained by applying an OR to its output and ~~the~~ an output of the selector (S81) of said first start-aligned conveyer circuit (651);

a lead bit position storage circuit (653) ~~that is configured of~~ comprising:

n flip-flops with hold (R1,..., Rn) that set at ~~the~~ a data input ~~the~~ an output of the conveyer circuits (CP1,, ..., CPn), fetch data for a former-half period of the clock (CK4T) and yet at ~~the~~ a time that ~~the~~ an output of said start-aligned control circuit (652) is under regulation, and hold in ~~the~~ other conditions; and

n flip-flops (Rn+1,..., R2n) that set at ~~the~~ a data input ~~the~~ an output of the conveyer circuits (CPn+1, ..., CP2n), fetch data for a latter-half period of the clock (CK4T) and yet at ~~the~~ a time that ~~the~~ an output of said start-aligned control circuit (652) is under regulation, and hold in ~~the~~ other conditions; and

wherein said alignment circuit (650) ~~includes~~ comprises:

an OR circuit group that applies an OR to ~~the~~ an output of ~~the~~ a free lead bit position storage circuit (653), and ~~the~~ an output of ~~the~~ an n-th lead bit position storage circuit (653) from the lead bit position of this lead bit position storage circuit (653),

n selectors (S91, S92,..., S9n) that select n bits starting with ~~the~~ a lead bit that ~~the~~ an output of this OR circuit group indicates from ~~the~~ an output of the 1:n de-multiplexer (640), further select for a former-half of the clock (CK4T) when ~~the~~ a lead bit is D1,..., Dn, and select

for a latter-half of the clock (CK4T) when the lead bit is Dn+1,..., D2n and D0; and

flip-flops (F91, F92,..., F9n) that sample n bits of ~~the~~ an output of these selectors (S91, S92,..., S9n) with ~~the~~ a back edge of the clock (CK3T), and

wherein said m-way n-bit multiplexer (670) fetches from ~~a~~ an m-address n-bit FIFO circuit (660) comprising:

a write address generation (661) that inputs into the first flip-flop a signal obtained by applying an AND to ~~the~~ negative outputs ~~of the~~ from first (m-1) flip-flops out of m flip-flops connected continuously, and applies an INPUT and an AND to the regulation control signal (strt) of said start-aligned control circuit (652) of said first start-aligned detection circuit (650) in inputting the first flip-flop or all flip-flops; and

a m x n FIFO (662) having ~~the~~ an address number m and ~~the~~ a bit number n that writes ~~the~~ an output of said alignment circuit (650) as ~~the~~ a data input according to ~~the~~ a write address, n-bit data written in said m x n FIFO (662) according to the write address; and

wherein said n-bit register (680) is n flip-flops (FD0, FD1, FD2, and FD3) that write ~~the~~ an output of said m-way n-bit multiplexer (670) with system clock (CLKSYS), and

wherein said second data processing circuit (700) ~~includes~~ comprises:

a second start-aligned conveyer circuit (751) that compares ~~the~~ an output of the 1:n de-multiplexer (740) of said second data processing circuit (700) with the second specific signal string as ~~the~~ an input;

a third start-aligned conveyer circuit (752) that compares ~~the~~ an output of the 1:n de-

multiplexer (740) of said second data processing circuit (700) with the third specific signal string as ~~the~~ an input; and

a regulation control circuit (753) comprising:

a flip-flop (FB4) that applies an AND to ~~the~~ an output of said second start-aligned conveyer circuit (751) and ~~the~~ an output of a plurality of flip-flops (FB2 and FB3) connected continuously, which obtain ~~the~~ a negative output delayed in inputting ~~the~~ a same output, and prepares the regulation start signal that is of a ~~differential~~ pulse waveform to distribute it to all said first data processing circuits (600); and

a flip-flop (FB1) that sets at ~~the~~ an input a signal obtained by applying an OR to a signal obtained by applying an AND to ~~the~~ a negative signal of the regulation start signal and the output of the flip-flop (FB1), and ~~the~~ an output of the selector (S81) of said third start-aligned conveyer circuit (752), and prepares ~~the~~ a regulation finish signal; and

wherein said read address generation circuit (770) sets at ~~the~~ an input of the first flip-flop a signal obtained by applying an AND to ~~the~~ a negative output of ~~the~~ first (m-1) flip-flops (FC2 to FC4) out of ~~the~~ m flip-flops (FC2 to FC5) connected continuously, applies an INPUT and an AND to ~~the~~ a read address start signal from ~~the~~ a synchronizing circuit (760) in inputting the first or all flip-flops, and distributes to all said first data processing circuit (600) ~~the~~ a read address prepared from ~~the~~ an output of the m flip-flops (FC2 to FC5), and

wherein, when ~~the~~ a time became maximized that: the first specific signal string and the third specific signal string were output simultaneously from said second transmitter circuit (300);

the first specific signal string was detected in said first start-aligned detection circuit (650) via said first transmitter circuit (200), a transmission line (800), a receiver (610), a sampler and 1:2 de-multiplexer (630) of said first data processing circuit (600), and the 1:n de-multiplexer (640); and

the signal string ranging ~~the~~ a next bit to n bits was extracted in said alignment circuit (650) and was written into said m-address n-bit FIFO circuit (660), even though ~~the~~ a time became minimized that:

the third specific signal string was detected as the third specific signal string in said second start-aligned detection circuit (750) via said second transmitter proc circuit (300), a transmission line (900), a receiver (710), a sampler and 1:2 de-multiplexer (730)of said second data ~~essing~~ addressing circuit (700), and a 1:n de-multiplexer (740);

the read address was generated via said synchronizing circuit (760) and said read address generation circuit (770); and

the data was written into said n-bit register (680) via said m-way n-bit multiplexer (670) by this read address, so that said m-address n-bit FIFO circuit (660) writes the data more later than the signal string reaches said n-bit register (680) via said m-way n-bit multiplexer (670), ~~the~~ a number of the flip-flops of said synchronizing circuit (760) was increased, when the time became minimized that: the first specific signal string was detected in the first start-aligned detection circuit (650) via said first transmitter circuit (200), a transmission line (800), a receiver (610), a sampler and 1:2 de-multiplexer (630) of said first data processing circuit (600) and the

1:n de-multiplexer (640); and

the bits starting with the next bit to the (m x n +1)th bit from the next bit, which was again written into the address o after circulation of the address of the m-address n-bit FIFO circuit (660), were extracted in said alignment circuit (650) and were written into the address 0 of said m-address n-bit FIFO circuit (660), even though the time became maximized that: the third specific signal string was detected as the third specific signal string in said second start-aligned detection circuit (750) via said second transmitter circuit (300), a transmission line (900), a receiver (710), a sampler and 1:2 de-multiplexer (730)of said second data processing circuit (700), and a 1:n de-multiplexer (740); the read address was generated via said synchronizing circuit (760) and said read address generation circuit (770); and

its read address was written into said n-bit register (680) via said m-way n-bit multiplexer (670), so that the m-address n-bit FIFO circuit 660 writes the n-bit data starting with the bit next to the first specific signal string more earlier than the signal string is written into said n-bit register (680) via said m-way n-bit multiplexer (670), the flip-flop number of said synchronizing circuit (760) was increased, and so as to satisfy two conditions, the address number of said m-address n-bit FIFO (660) was set at m.

18. (Currently amended) The high-speed transmission system having a low latency according to claim 17, wherein said second start-aligned conveyer circuit (751) comprises:

a an n-input OR circuit that sets the second specific signal string at all signal strings

including 1, and applies an OR to all output of said 1:n de-multiplexer (740) of said second data processing circuit (700).

19. (Original) The high-speed transmission system having a low latency according to claim 18, wherein selectors (S91, ..., S9n) of said alignment circuit (650) of said first data processing circuit (600) are controlled so that selectors (S91, ..., S9n) are valid when the regulation control signal (strt) of said alignment circuit (650) was set, and they are invalid when it was reset.

20. (Currently amended) The high-speed transmission system having a low latency according to claim 17, further ~~including~~ comprising:

a first analogue PLL circuit (100) that distributes to said first transmitter circuit (200) and said second transmitter circuit (300) a clock for transmission having ~~a~~ an n/2 multiple frequency, which was synchronized with the system clock (CLKSYS); and

~~including~~ a second analogue PLL circuit (500) that distributes to said first data processing circuit (600) and said second data processing circuit (700) a clock for transmission having ~~a~~ an n/2 multiple frequency, which was synchronized with the system clock (CLKSYS).

21. (Currently amended) The high-speed transmission system having a low latency according to claim 20, wherein said first analogue PLL circuit (100), in which the system clock (CLKSYS) in the send side and the system clock (CLKSYS) in the receive side thereof are a synchronized

clock, sets at a REF clock input the system clock (CLKSYS) or a signal having ~~the~~ a same or a 1/integer frequency , which has a given phase relation with the system clock (CLKSYS), said first analogue PLL circuit (100) ~~including~~ comprising:

a voltage control-type variable frequency oscillator (120) that oscillates at ~~a~~ an n/2 multiple frequency of the system clock (CLKSYS);

a counter (130) that divides, when an output of this voltage control-type variable frequency oscillator (120) is ~~a~~ an n/2 multiple frequency of the system clock (CLKSYS), so that ~~the~~ an output has ~~the~~ a same frequency as the system clock (CLKSYS); and

a phase comparator (110) that makes a phase comparison between ~~the~~ an output of this counter(130) and ~~the~~ a REF clock to control a control voltage of said voltage control-type variable frequency oscillator (120) so that ~~the~~ phases of ~~the~~ an output of said counter(130) and ~~the~~ a frequency of the REF clock become the same.

22. (Currently amended) The high-speed transmission system having a low latency according to claim 21, wherein in said first data processing circuit (600) and in said second data processing circuit (700) is omitted the second analogue PLL circuit (500) distributing the clock for transmission having ~~a~~ an n/2 multiple frequency, which was synchronized with the system clock (CLKSYS), and

wherein ~~the~~ an output of the first analogue PLL circuit (100) in the send side is distributed to said first data processing circuit (600) and said second data processing circuit (700) via ~~the~~ a

driver (140), ~~the~~ a transmission line (1000), and ~~the~~ a receiver(540) as ~~the~~ a clock for transmission having ~~a~~ an n/2 multiple frequency, which was synchronized with the system clock (CLKSYS).

23. (Original) The high-speed transmission system having a low latency according to claim 22, wherein the system clock (CLKSYS) in the send side and the system clock (CLKSYS) in the receive side are not synchronized.

24. (Currently amended) The high-speed transmission system having a low latency according to claim 17, wherein said pre-emphasis control circuits (230 and 330) ~~are configured of~~ comprise:

a flip-flop (F43) that samples and fetches ~~the~~ a positive output of the flip-flop (F40) of said n/2:1 multiplexer (220 and 320) with ~~the~~ a leading edge of the sampling clock (CK41);

a flip-flop (F44) that samples and fetches ~~the~~ a positive output of the flip-flop (F41) with ~~the~~ a back edge of the sampling clock (CK41) and yet at ~~the~~ a next cycle; and

selectors (S42 and S43) that select ~~the~~ a positive output and ~~the~~ a negative output of the flip-flop (F44) for a former-half period by setting an inverse signal of the sampling clock (CK41) at ~~the~~ a selection signal and obtains ~~the~~ a positive output and ~~the~~ a negative output of the flip-flop (F43) for a latter-half period, and

wherein, to ~~the~~ selectors (S40 and S41) which select the positive output and the negative output of the flip-flop (F40) for a former-half period and select the positive output and the

negative output of the flip-flop (F42) for a latter-half period as a normal output signal, is output the output with an output amplitude of the drivers (240 and 340) is increased when ~~the~~ a negative output of the selector (S42) is ~~the~~ a same as the positive output of the selector (S40), and the output with the output amplitude is reduced when it is different, and yet selection can be made from a plurality of pre-emphasis quantity, including no change in a magnitude of the amplitude.